UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,712	04/14/2004	Jae-Bon Koo	6161.0122.US	5230

58027 7590 01/05/2006

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 01/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,712	KOO ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *11 and 19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *JPO Abstract*.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 1-10 and 12-18, in the reply filed on December 9, 2005 is acknowledged.

Specification

2. The disclosure is objected to because of the following informalities: on page 10, line 3 of the specification, the typographical error "illustratedthe" is found.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 13 recites the limitation "the silicon layers having low current mobilities" in lines 8-9. There is no previous reference to silicon layers that have low current mobilities in either claim 13 or claim 12. Thus there is insufficient antecedent basis for this limitation in the claim.

5. Claim 18 recites the limitation "the silicon layer having low current mobility" in lines 3-4. There is no previous reference to a silicon layer that has low current mobility in claim 18, claim 14 or claim 12. Thus there is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Insofar as definite, claims 1-10, 12, 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada '025 in view of Zhang et al. '733.

a. Regarding claims 1-5, 7, 12 and 14-18, Yamada discloses a flat panel display comprising a plurality of pixels, each of the pixels including R, G, and B unit pixels to embody red, green, and blue colors (fig. 3); each of the unit pixels including a light-emitting device (fig. 5, 160); transistors of the same channel size made of polycrystalline silicon (fig. 5 is representative of R, G, and B pixels, all having the same size control transistor) to control currents supplied to the LED of each unit pixel (40); and transistors to switch on or off each unit pixel (30). The reference discloses that the light emission efficiency of the layers that emit different colors of light varies with each layer, and that a larger current must be supplied to the low emission efficiency layer than the current that is supplied to the high emission efficiency layer in order to achieve white balance (col. 3, lines 1-8).

Yamada does not teach using transistors with different current mobilities to supply different levels of current to the light emission layers. Zhang et al. teaches a flat panel display comprising a plurality of pixels, wherein the unit pixels have transistors formed by metal induced crystallization of high mobility (high crystallinity) and low mobility (lower

crystallinity and/or amorphous) to adjust the level of current received by the pixels (col. 3, lines 19-31; col. 3, line 67 - col. 4, line 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the current-varying transistors of different mobility of Zhang et al. to drive the color pixels of Yamada that require varying current in order to achieve white balance, wherein the high mobility transistor would be connected to the low emission efficiency layer and the low mobility transistor would be connected to the high emission efficiency layer. One would have been motivated to do this because it was well known that the varying emission efficiency of RBG pixels can be compensated by varying the drive current to each unit pixel (Yamada, col. 3, lines 1-8), allowing the flat panel display to perform its intended function of producing white light. Also, the device of Zhang et al. allows for transistors of differing mobility (differing current) to be produced on the same substrate (Zhang et al., col. 3, line 67 - col. 4, line 1), thus making the manufacturing process faster and more simple.

b. Regarding claims 6, 8, 9 and 10, all of the elements of the claims are taught by Yamada in view of Zhang et al. as discussed above. The process limitations of forming the polycrystalline silicon by either the metal induced crystallization (MIC) method or by the metal induced lateral crystallization (MILC) method found in these product claims invoke the product-by-process doctrine. Product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps (*MPEP § 2113*). For

example, anticipation of these claims does not require either MIC or MILC to result in the polycrystalline silicon film as claimed.

8. Insofar as definite, claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada '025 in view of Zhang et al. '733, and further in view of Yamada, Japanese Patent '399.

Yamada '025 in view of Zhang et al. teaches all of the elements of the claim as discussed above, but does not teach the transistors of the unit pixels to have different channel lengths. Yamada '399 teaches a flat panel display comprising a plurality of pixels, each of the pixels including R, G and B unit pixels, and each unit pixel having a transistor of different channel length to vary the current supplied to the unit pixel, thus achieving white balance between the color pixels having different light emission efficiency (abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the transistors of varied channel length of Yamada '399 in the flat panel display of Yamada '025 in view of Zhang et al. One would have been motivated to do this because varying the channel length would further enhance the ability to control the current supplied to the unit pixels, thus achieving greater balance of white light and increasing the performance of the device.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Yamazaki '565, Kim et al. '819, Cok et al. '549, and Nakamura et al. '328 disclose flat panel displays comprising a plurality of pixels, each pixel including R, G, and B unit pixels to achieve white balance.

b. Joo et al. '130 and Takemura '716 disclose flat panel displays having control transistors formed by metal induced crystallization to create channels of varying crystallinity and mobility.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sjf
12/22/05

BRADLEY K. SMITH
PRIMARY EXAMINER